

# TOSHIBA MOS MEMORY PRODUCTS

**256K BIT (32K WORD × 8 BIT) MASK ROM**  
N-CHANNEL SILICON GATE

**TMM23256P**

020668

## DESCRIPTION

The TMM23256P is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, thus being most suitable for use in character generator.

Consisting of static memory cells and clocked peripheral circuitry, the TMM23256P provides a high speed and low power dissipation (access time 150ns, operating current 40mA).

The TMM23256P also features an automatic stand-by power mode. When deselected by Chip Enable ( $\overline{CE}$ ), the operating current is reduced from 40mA to

10mA. Output Enable ( $\overline{OE}$ ) is effective in preventing data confliction on a common bus line.

The TMM23256P uses the address latch system that the falling edge of  $\overline{CE}$  latches all inputs except for  $\overline{OE}$ , thus can be easily connected to a system where address and data buses are commonly used.

The TMM23256P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production on high performance.

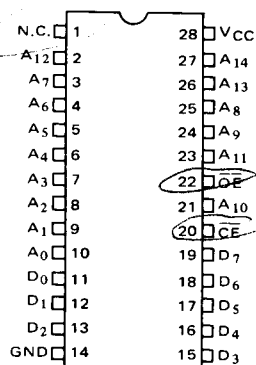
The TMM23256P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

## FEATURES

- Single 5V Power Supply
- Fast Access Time : 150ns (Max.)
- Low Power Dissipation
  - Average Current : 40mA (Max.)
  - Standby Current : 10mA (Max.)
- Inputs protected : All Inputs have Protection Against Static Charge

- Edge Enabled Operation :  $\overline{CE}$
- Output Buffer Control :  $\overline{OE}$
- Input and Output : TTL Compatible
- Three State Outputs : Wired OR Capability
- 28 pin Standard Plastic DIP

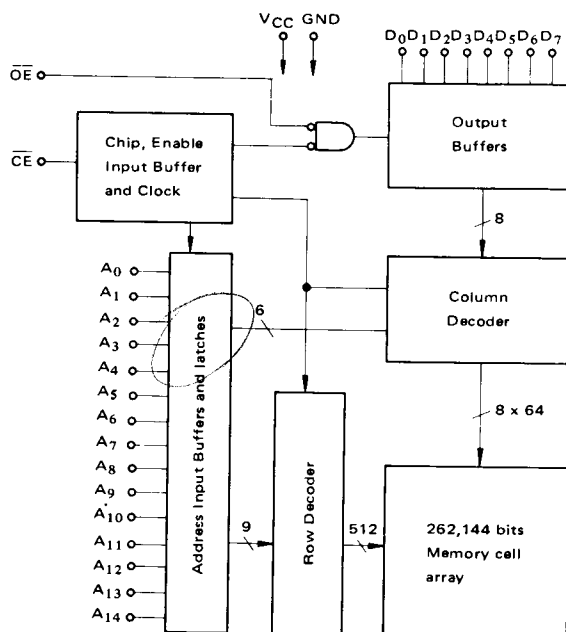
## PIN CONNECTION



## PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$D_0 \sim D_7$	Data Outputs
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
N.C.	No Connection
$V_{CC}$	Power Supply Terminal
GND	Ground

## BLOCK DIAGRAM



# TMM23256P

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
$V_{CC}$	Power Supply Voltage	$-0.5 \sim 7.0$	V
$V_{IN}, V_{OUT}$	Input and Output Voltage	$-0.5 \sim 7.0$	V
$T_{OPR}$	Operating Temperature	$0 \sim 70$	°C
$T_{STRG}$	Storage Temperature	$-55 \sim 150$	°C
$T_{SOLDER}$	Soldering Temperature · Time	$260 \cdot 10$	°C · sec
$P_D$	Power Dissipation ( $T_a = 70^\circ\text{C}$ )	1.0	W

## D.C. OPERATING CONDITIONS ( $T_a = 0 \sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IH}$	Input High Voltage	—	2.2	—	$V_{CC} + 1$	V
$V_{IL}$	Input Low Voltage	—	-0.5	—	0.8	V
$V_{CC}$	Power Supply Voltage	—	4.5	5.0	5.5	V

## D.C. and OPERATING CHARACTERISTICS ( $T_a = 0 \sim 70^\circ\text{C}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{IH}$	Input High Current	$V_{IN} = 5.5\text{V}$	—	0.05	10	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{IN} = \text{GND}$	—	-0.05	-10	$\mu\text{A}$
$V_{OH}$	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	3.3	—	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 3.2\text{mA}$	—	0.3	0.4	V
$I_{LOH}$	Output Leakage Current	$V_{OUT} = 5.5\text{V}$	—	0.05	10	$\mu\text{A}$
$I_{LOL}$		$V_{OUT} = 0.4\text{V}$	—	-0.1	-20	$\mu\text{A}$
$I_{CC1}$	Standby Current	$\overline{CE} = 2.2\text{V}$	—	—	10	mA
$I_{CC2}$	Average Current	$t_{CYC} = 230\text{ns}, I_{OUT} = 0\text{mA}$	—	—	40	mA

- Typical values are at  $T_a = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

## CAPACITANCE ( $T_a = 25^\circ\text{C}, f = 1\text{MHz}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = \text{A.C. GND}$	—	5	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = \text{A.C. GND}$	—	8	15	pF

Note : This parameter is periodically sampled and is not 100% tested.

## A.C. CHARACTERISTICS

(Ta = 0 ~ 70°C, V<sub>CC</sub> = 5V ± 10%)

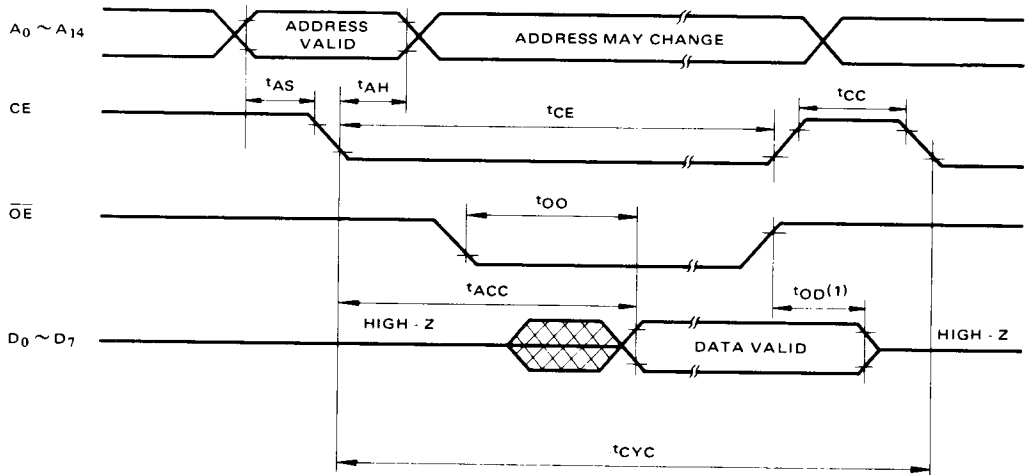
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t <sub>CE</sub>	CE pulse width	—	150	—	—	ns
t <sub>AS</sub>	Address Setup Time	—	0	—	—	ns
t <sub>AH</sub>	Address Hold Time	—	30	—	—	ns
t <sub>ACC</sub>	Access Time	—	—	—	150	ns
t <sub>OO</sub>	Output Delay Time form OE	—	—	—	70	ns
t <sub>OD</sub>	Output Turn off Delay	—	—	—	70	ns
t <sub>CC</sub>	CE off Time	—	70	—	—	ns
t <sub>CYC</sub>	Cycle Time	t <sub>AS</sub> = 0ns, t <sub>r</sub> , t <sub>f</sub> = 5ns	230	—	—	ns

- Typical values are at Ta = 25°C and V<sub>CC</sub> = 5V.

## A.C. TEST CONDITIONS

- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5ns
- Input Pulse Levels : 0.8 ~ 2.4V
- Timing Measurement Reference Levels : Input : 1V and 2.2V  
Output : 0.8V and 2.0V

## TIMING WAVEFORMS



Note (1) t<sub>OD</sub> is specified from OE or CE, whichever occurs first.

# TMM23256P


## OPERATION INFORMATION

The TMM23256P has two control functions.

The chip enable ( $\overline{CE}$ ) controls the operation power and should be used for device selection. The falling edge of the  $\overline{CE}$  will activate the device and latch the addresses. The output enable ( $\overline{OE}$ ) control the out-

put buffers, independent of device selection. Assuming that  $\overline{OE} = V_{IL}$ , the output data is valid at the outputs after  $t_{ACC}$  (150ns) from the falling edge of the  $\overline{CE}$ .

The operation modes of the TMM23256P are listed in the following table.

MODE	$\overline{CE}$	ADDRESS	$\overline{OE}$	OUTPUT	POWER
Standby	H	*	*	High Impedance	Standby
Latch		Valid	*	High Impedance	—
Read	L	**	L	Data Out	Active
Output Deselect	L	*	H	High Impedance	Active

Note \* : Don't care

\*\* : Address may change after  $t_{AH}$ .

## APPLICATION INFORMATION

### 1. POWER SUPPLY DECOUPLING

The operating current  $I_{CC}$  waveforms for TMM23256P are shown in Fig. 1, 2.

The TMM23256P is a clocked device, so the transient current peaks are produced on the  $\overline{CE}$  transition and  $\overline{CE}$  active level.

The  $I_{CC}$  current transients require adequate decoupling of  $V_{CC}$  power supply.

### 2. POWER ON

The TMM23256P requires initialization prior to normal operation. Two initialization methods are as follows:

- (1) A minimum 100 $\mu$ s time delay is required after the application of  $V_{CC}$  (+5V) before proper device operation is achieved. And during this period,  $\overline{CE}$  must be at  $V_{IH}$  level.
- (2) A minimum 100 $\mu$ s time delay is required after the application of  $V_{CC}$  (5V), and then a minimum of one initialization cycle must be performed before proper device operation is achieved.

Initialization cycle : An initialization cycle is one Chip Enable clock cycle from the first down edge of the  $\overline{CE}$  till the next down edge.

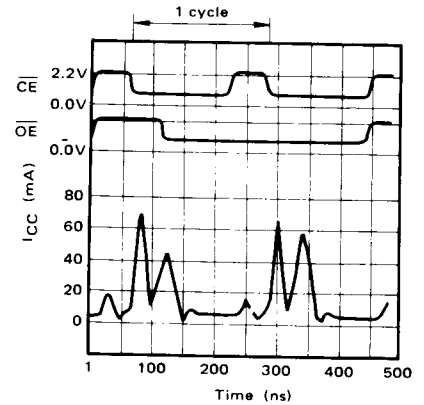


Fig. 1  $I_{CC}$  vs. Time (1)

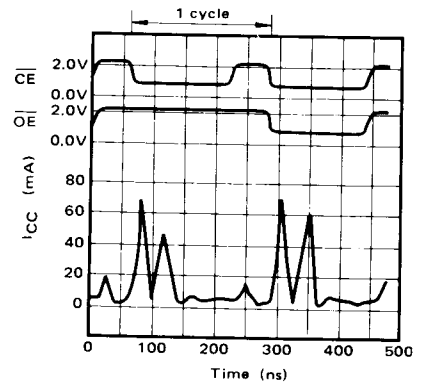
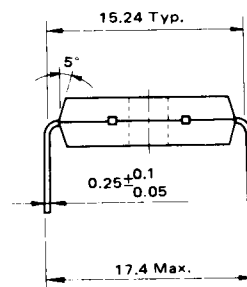
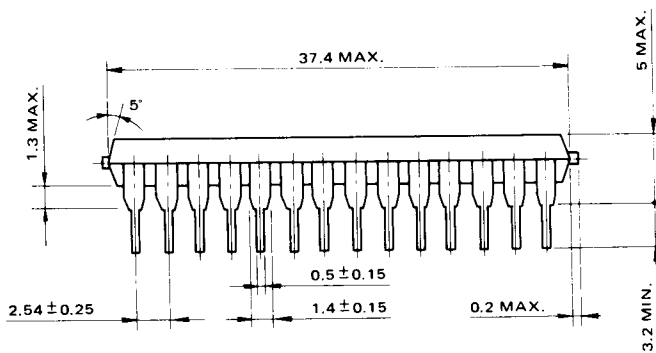
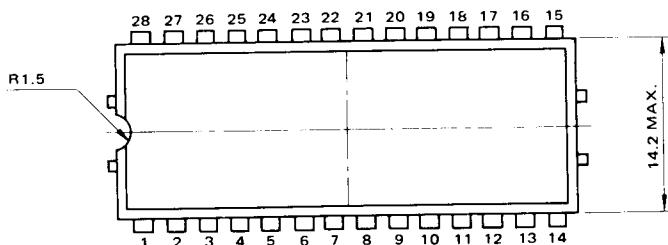


Fig. 2  $I_{CC}$  vs. Time (2)

# TMM23256P

## OUTLINE DRAWINGS

Unit : mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.